IOSR Journal of Electrical and Electronics Engineering (IOSR-JEEE)
e-ISSN: 2278-1676,p-ISSN: 2320-3331,
PP 66-72
www.iosrjournals.org

Three State Switching Cell Based Boost Converter For Single Phase Full Bridge Inverter Application

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Abstract *: This paper presents a dc-dc boost converter and dc-ac inverter combination. Dc-dc boost converter topology is based on the three state switching cell with high voltage gain. The converter section is analyzed considering the operation in continuous conduction mode and in the overlapping mode. The converter section supplies input to a single phase full bridge inverter with sinusoidal pulse width modulation control. The closed loop PI control for the converter section adds to its advantages. Both the advantages of the converter and inverter section are combined in the proposed topology. Several topologies where high voltage dc-dc conversion and dc- ac inversion are initially investigated. Comparison of the control system is done before selecting the control for the converter section. The simulated results are presented to validate the theoretical analysis.*
Keywords *- Boost converter, High voltage gain, PI control, Single phase full bridge inverter, Three state switching cell.*

I. Introduction

Several types of applications such as uninterruptible power systems (UPS) and adjustable-speed drives often demand the low dc voltage from batteries, photovoltaic panels, fuel cells and small wind turbines to be stepped up. Typical low voltages range from 12 to 125 V must be increased to 300 or 440 V so that a high voltage dc bus is obtained.

Inverters are commonly used device in today’s society. They are often used to take a low voltage DC source, such as the battery in a motor vehicle, and supply a high volt ac source running at 50 Hz. Since the market for such a product is so large, many competitors have entered with various implementations. Cheap designs use a “modified sine wave” which looks like a square wave. Although this is able to power devices which need the high volts about 120 volts, substantial amounts of noise are introduced into the circuits. This introduced noise is highly undesirable with audio devices. To avoid this problem, a true sine wave must be generated from the DC source. Such products exist in the market, but have a high cost associated with them. In an attempt to lower costs, a method of generating a pure sine wave with Pulse Width Modulation is being implemented. One stipulation to using Pulse width modulation is the assumption that the source voltage be larger than the output voltage. This introduces a need for a DC-DC converter which can provide the inverter with a high voltage source i.e, if the desired output of the inverter is 300 to 400 volts, the DC-DC converter must supply about 400 volts consistently.

The existing dc-dc converter topologies were studied to arrive at a better selection of the dc-dc converter with high voltage gain for the proposed topology.

The connection of several boost converters in cascade[1] would be a possible solution for the problems raised by a conventional boost converter. Even then, increased complexity and reduced efficiency are serious drawbacks in this case.

Conventional push pull converter [2] is adequate for low power application and low input voltages. Since the voltage stress across the main switches is twice the input voltage. Other drawbacks include the leakage inductance of the transformer, responsible for high voltage peaks across the switch during turn on to turn off switching transition.

In boost converter with two inductors and an auxiliary transformer [3], source and the load are not connected to the same reference node. A novel version of the structure introduced in [4] have same reference node and can generate an output voltage four time that of input voltage. However it is worth to mention that converter topology mentioned above has its whole load current flowing through the capacitors, thus compromising robustness and reliability.

An interleaved boost converter with multiplier capacitors is proposed in [5]. This arrangement is analogous to the series capacitors used in SEPIC converter, but allowing the static gain to increase. Even though it is recommended for high current applications where the input current ripple is reduced and the voltage stress across the switches is half of the total output voltage, the high current through the series capacitors may cause efficiency to decrease in high power applications.

A novel family of dc-dc converters using 3SSC and voltage multiplier cells was introduced in [6], while significant advances have been achieved in terms of reduced voltage stress across the main switches, reduced input ripple current, minimization of size, weight and volume associated to magnetic, reduced switching losses and high efficiency over the entire load range. However, the reduced useful life of series capacitors and high component count can be pointed out as the drawbacks.

Considering all the above mentioned problems, a non isolated dc-dc boost converter based on 3SSC with high voltage gain [7] is introduced in the converter section of the proposed topology. The detailed description and advantage are mention in this paper.

This paper introduces DC-AC converter system which comprises of two sections in which first section includes a dc-dc converter section and the second one includes an inverter section. The block diagram of the proposed topology is show in the fig.1.

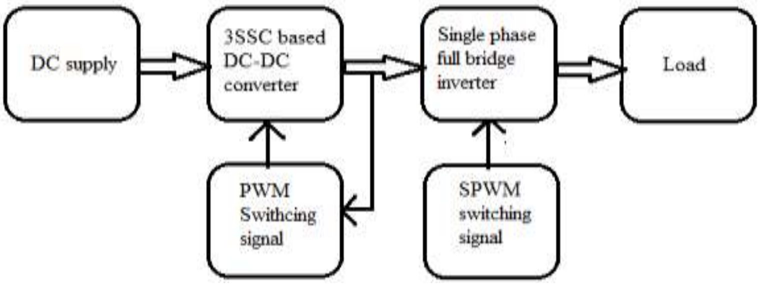

Fig.1.Block diagram of the proposed topolgy

II. PROPOSED TOPOLOGY

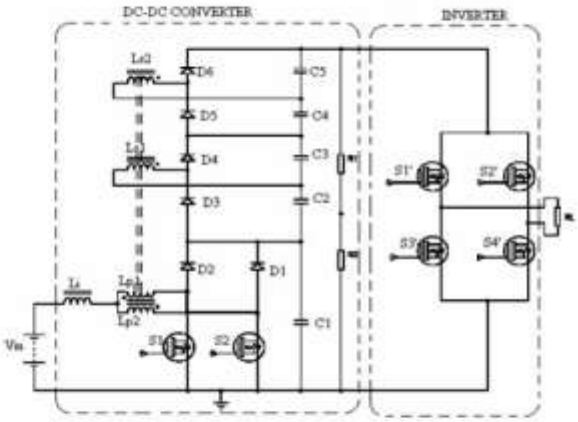

Fig.2. Circuit diagram of the proposed topolgy

The fig.2 shows the circuit diagram of the proposed topology in which the proposed converter is a high voltage gain boost converter based on 3SSC.The converter is composed by the following elements: input voltage V_{in} ,inductor L_i ,transformer connected to active switches S1and S2,rectifier diodes D1,D2,D3,D4,D5 and D6, auxiliary clamping capacitors C_1,C_2,C_3,C_4 and C_5.R_1,R_2 are used as the potential divider resistors for feedback voltage. Filter capacitors are also used to reduce the ripple in the dc output voltage of the converter. DC-AC inverter section consists of four switches S_1’,S_2’,S_3’&S_4’which forms a single phase full bridge inverter. Filter capacitor and inductor are also used at the output of inverter section.

2.1. DC-DC converter section

The operating stages of the boost converter are determined by the current flowing through L_i. Even though converter is able to operate in continuouse conduction mode(CCM), discontinuouse conduction mode (DCM) or critical conduction mode (CRM) with both conditions given by D>0.5 in overlapping mode(OM) or

D<0.5 in non overlapping mode(NOM), the qualitative analysis is supposed to be developed for CCM-OM as follows.

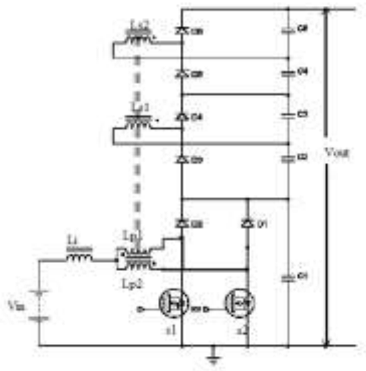

Fig.3.Circuit diagram of the DC-DC converter section

The circuit diagram that represents the DC-DC converter section is shown in the fig.3.The operation of converter for one switching cycle is described in the table shown below.

TABLE I: The operation of converter for one switching cycle

STAGES	S_1	S_2	D_1	D_2	D_3	D_4	D_5	D_6
I(t_0,t_1)	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF
II(t_1,t_2)	OFF	ON	OFF	ON	ON	OFF	ON	OFF
III(t_2,t_3)	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF
IV(t_3,t_4)	ON	OFF	ON	OFF	OFF	ON	OFF	ON

The static gain expression for the converter can be defined as:

$$G_v = \frac{Vbus}{Vbat} = \frac{Vo}{Vin} = \frac{1}{(1-D)}.\ (1+ \sum_{j=1}^{n} aj\ ) \quad (1)$$

where,

$$a_j = \frac{Nsj}{Np} \quad (2)$$

where j is the number of secondary windings. Besides, the dimensionless quantity a_j represents the ratio between the number of turns for a given secondary winding j represented as N_{sj} and the number of turns for the primary winding N_p.

The main characteristics of the topology are:

- Operation at high switching frequency
- The input inductor is designed for twice such frequency, in order to minimize weight and volume.
- Voltage stress across the switches is lower than half the output voltage and naturally clamped by one output capacitor, allowing the use of MOSFET transistors with reduced intrinsic on-resistance.
- The input current presents small ripple.
- The output voltage can be further stepped up by increasing the transformer turns ratio without compromising the voltage stress across the switches.
- The output voltage is naturally balanced thus making the converter suitable for supplying single phase inverter.

2.2. Inverter section

In the inverter section the high voltage dc output from the converter section is fed to the inverter as its dc input. Thus, the single phase full bridge inverter converts the high voltage dc to single phase ac voltage .Filter circuits are used at the output of inverter. The fig.4., shows the circuit diagram of single phase full bridge inverter.

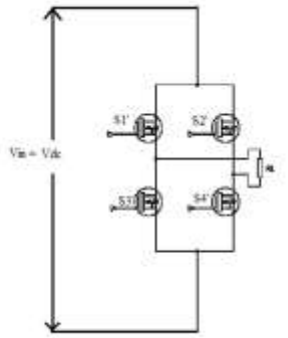

Fig.4.Circuit diagram of single phase full bridge inverter

The switching scheme used for the inverter section is shown in the table given below.

TABLE II: The switching scheme for inverter

S_1’	S_2’	S_3’	S_4’	OUTPUT
ON	OFF	OFF	ON	V_O
OFF	ON	ON	OFF	- V_O
ON	OFF	ON	OFF	0
OFF	ON	OFF	ON	0

The rms value of output voltage:

$$V_o = V_s \sqrt{\frac{p\delta}{\pi}} \quad (3)$$

Where,

V_s= source voltage
p= no:of pulses
δ=pulse width

III. CONTROL STRATEGY

The two different control systems are open loop and closed loop control. Closed loop control schemes are more accurate than open loop system. They are equally accurate and are not disturbed in the presence of non-linearities. Since they are composed of a feedback mechanism, so they clear out the errors between input and output signals, and hence remain unaffected to the external noise sources. Because of these advantages of the closed loop control is used in the dc-dc converter section of the proposed topology.

The closed loop PI controller is used in the proposed converter to achieve the desired output voltage. The PI controller continuously calculates an error value as the difference between a measured process variable and a desired set point. The controller attempts to minimize error over time by adjustment of a control variable. PI controllers are fairly common, since derivative action is sensitive to measurement noise.

The above mention PI closed loop control scheme is used by the converter section whereas the inverter section uses sinusoidal pulse width modulation to generate pulses for inverter.

In the SPWM modulation technique, multiple numbers of output pulse per half cycle and pulses of different width are generated. The width of each pulse is varying in proportion to the amplitude of a sine wave evaluated at the centre of the same pulse. The gating signals are generated by comparing a sinusoidal reference with a high frequency triangular signal.

Main advantages of using SPWM inverter:

- Low power consumption.
- High energy efficient up to 90%.

- High power handling capability.
- No temperature variation and ageing caused drifting or degradation in linearity.
- Easy to implement and control.
- Compatible with today's digital microprocessors

The PWM switching can be divided into two switching scheme which are PWM with Bipolar voltage switching and PWM with Unipolar voltage switching .In which SPWM with Unipolar voltage switching scheme has better harmonic profile compare to Bipolar voltage switching and hence SPWM with unipolar voltage switching is used for the single phase full bridge inverter.

IV. SIMULATION RESULTS

The proposed topology is designed for a dc voltage input of 48V to obtain an ac output voltage of 400V. The simulation circuit of the proposed topology is shown in the fig.5. Specifications used for dc-dc converter and inverter section is shown in the table given below.

TABLE III: Design specifications of the dc-dc converter

Parameter	Specification
Rated output power	P_{bus} =1000W
Rated input voltage	V_{in} =48V
Output voltage	V_O =400V
Switching frequency	f_s = 25KHz
Ripple current through inductor L_1	ΔI_{Li} =20% $I_{Li(avg)}$
Ripple voltage across auxiliary and output capacitors	$\Delta V_{c1\ldots c5} = \Delta V_{c01} = \Delta V_{C02}$=1%Vo
Number of secondary windings	j =2
Turns ratio of the transformer	$a_1=a_2=a=1$
Expected theoretical efficiency	η =93%

TABLE IV: Design specifications of inverter

Parameter	Specification
Rated output power	P_{bus} =100W
Rated input voltage	V_{dc}=400V
Rated output voltage	V_{acpeak}=400V
Switching frequency	fs=25khz
Filter capacitor and inductor	C_f=.215mH;L_f=470μF
Expected efficiency	η =90%

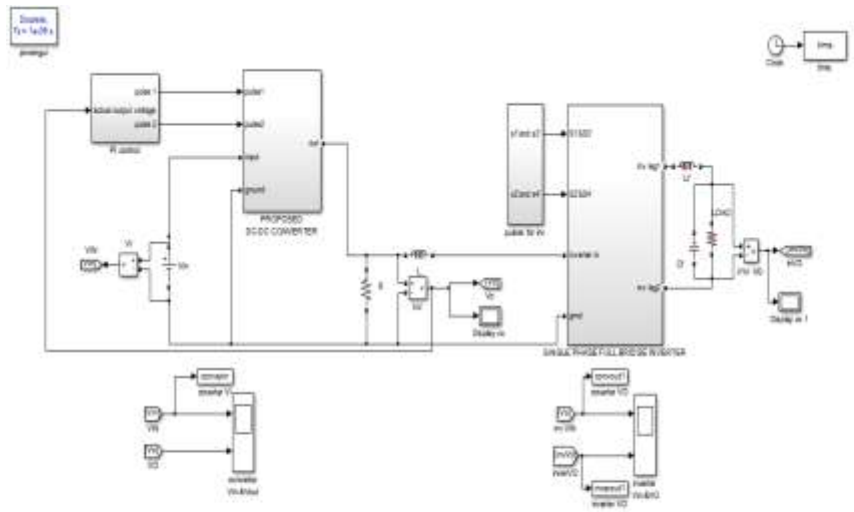

Fig.5.Simulation circuit of the proposed topology

Control scheme for the dc-dc converter section is decided after a comparison of output voltages obtained from the open loop and closed loop simulation results (fig.6). It is observed that closed loop PI control is more efficient than the open loop control scheme.

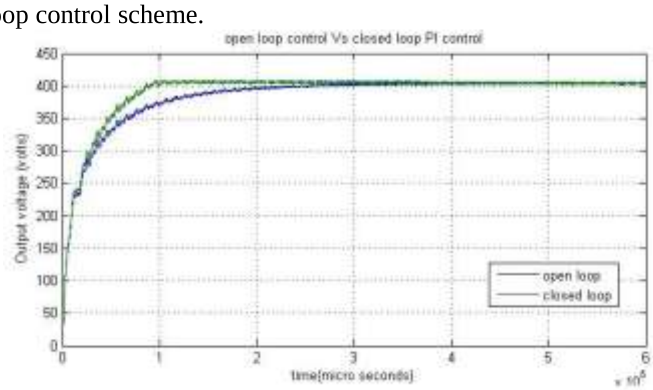

Fig.6.Comparison of the output voltages of the open loop and closed loop controlled dc-dc converter section.

The fig.7 shows the dc input voltage and dc output voltage of the converter section and the ac output voltage from the inverter section.

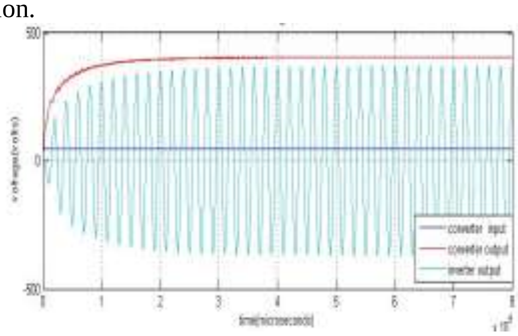

Fig.7.Input and output voltage waveform of the propose topology

V. CONCLUSION

This work has presented a combination of dc-dc converter with inverter, for high voltage application. The dc-dc converter is a non isolate boost converter based on 3SSC with high voltage gain. The inverter is single phase SPWM full bridge inverter. The advantages of both sections add the need for the proposed topology.

Advantages of DC-DC converter:

- Operation at high switching frequency
- The input inductor is designed for twice such frequency, in order to minimize weight and volume.
- Voltage stress across the switches is lower than half the output voltage and naturally clamped by one output capacitor, allowing the use of MOSFET transistors with reduced intrinsic on-resistance.
- The input current presents small ripple.
- The output voltage can be further stepped up by increasing the transformer turns ratio without compromising the voltage stress across the switches.
- The output voltage is naturally balanced thus making the converter suitable for supplying single phase inverter

Advantages of Inverter:

- Low power consumption.
- High energy efficient up to 90%.
- High power handling capability.
- No temperature variation-and ageing-caused drifting or degradation in linearity.
- Easy to implement and control.
- Compatible with today's digital microprocessors

The draw back in the proposed topology is the high voltage stress across the inverter section. Further investigations are being carried out to overcome this problem.

The proposed topology is recommended for high dc voltage and ac voltage applications

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